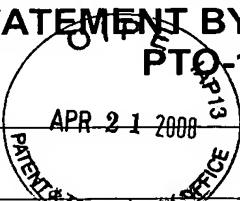


**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS**  
**PTO-1449**



Attorney Docket No.  
2885/76

Serial No.  
10/757,900

Applicant(s)  
Vorbach et al.

Filing Date  
January 14, 2004

Group Art Unit  
2117

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,659,797	August 19, 1997	Zandveld et al.			
	5,844,422	December 1, 1998	Trimberger et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,185,731	February 2001	Maeda et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,633,181	October 2003	Rupp			
	6,874,108	March 2005	Abramovici et al.			
	7,249,351	July 2007	Songer et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1 061 439	December 20, 2000	EPO				
	WO 01/55917	August 2, 2001	PCT				
	WO 02/071196	September 26, 2002	PCT				

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Albaharna, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.
	Schmidt, H. et al., "Behavioral synthesis for FGPA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS**  
**PTO-1449**

Attorney Docket No.  
2885/76

Serial No.  
10/757,900

Applicant(s)  
Vorbach et al.

Filing Date  
January 14, 2004

Group Art Unit  
2117

EXAMINER'S  
INITIALS

AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.